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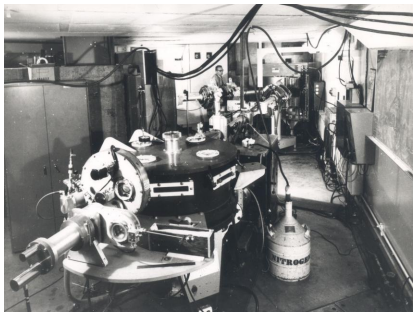
Satellites and System Design



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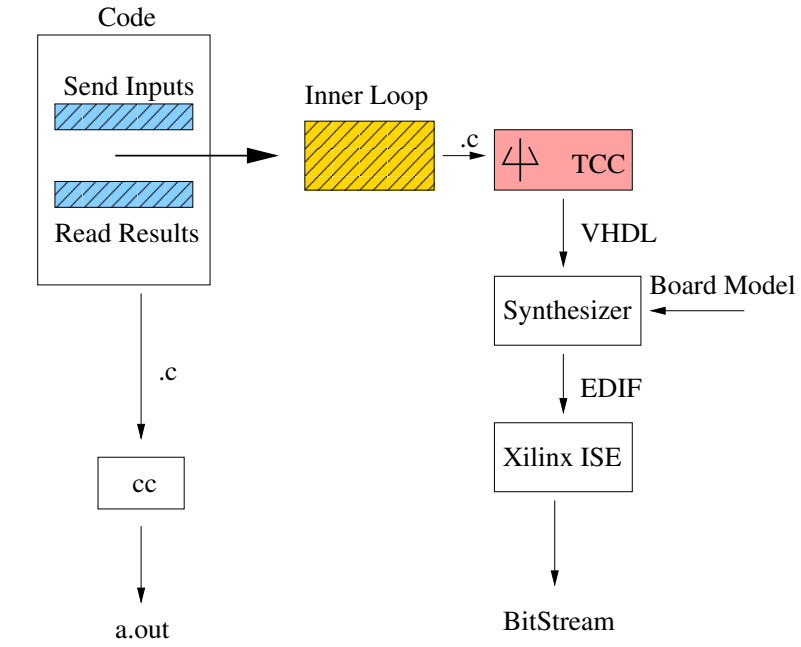
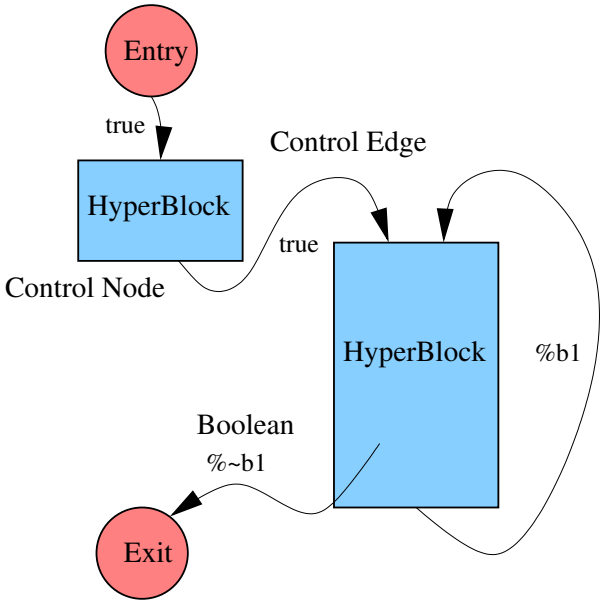
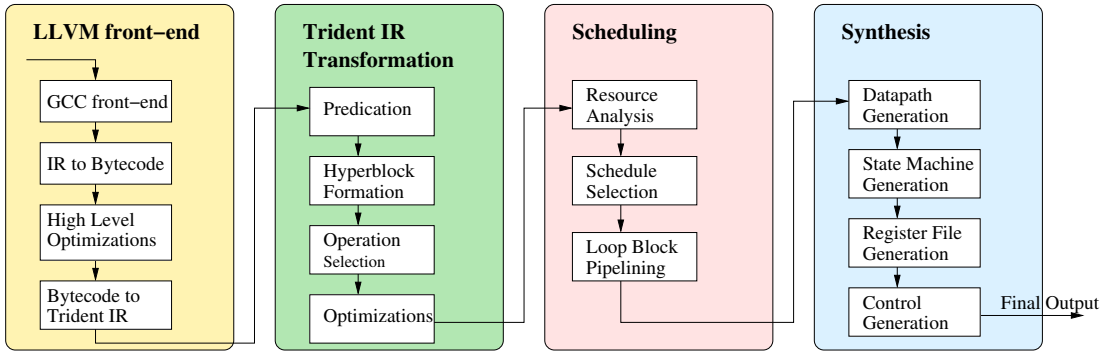
Los Alamos National Laboratory

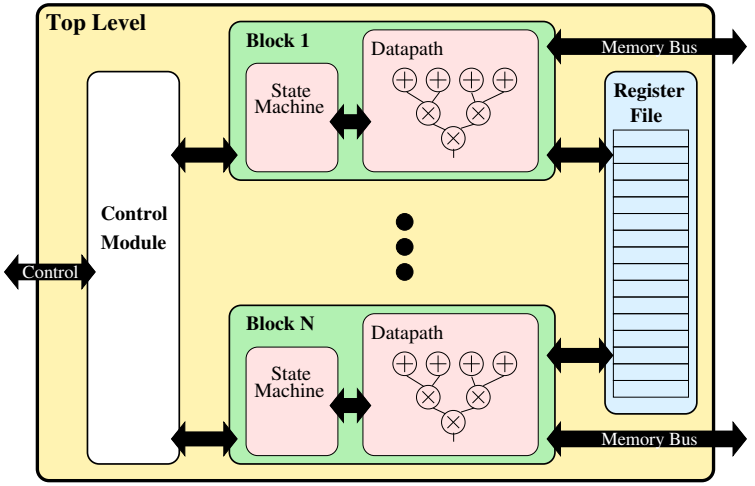
July 2015

Trident Compiler







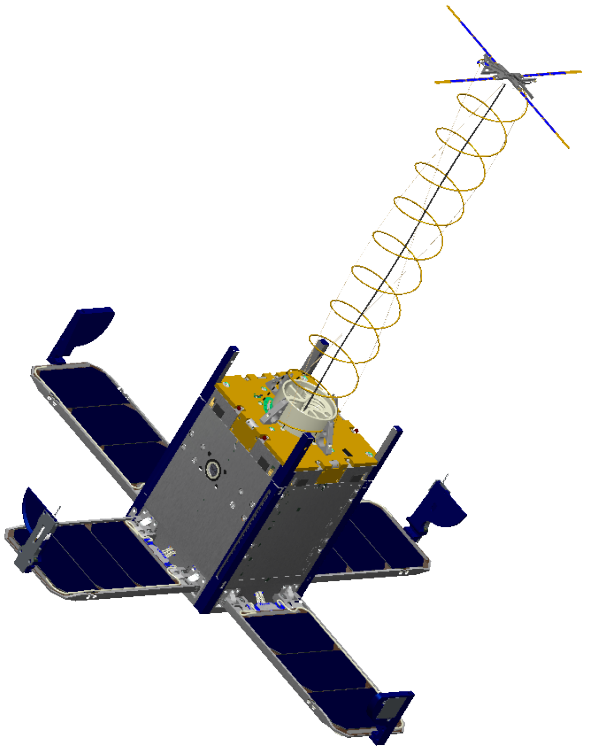


Cubesat Project

- Approached to work on Prometheus Project (Oct 2012)
- Prometheus is a second generation Cubesat developed at LANL
- They are testing low-cost development and operations methodologies as well as utility.
- The project had a short deadline, and was to be launched in April (2013).
- Asked to finish three things:
  - ⋆ Radio Control Interface
  - ⋆ Spartan FPGA programming
  - ⋆ Bitstream Scrubber for Spartan FPGA

Cubesat

- Several satellites work in a cluster
- Consists of four circuit boards and a backplane, 1.5U
- Two different antennas to one high frequency analog radio
- Two digital radio boards for processing
- Command and Control board
- Sensor and motor control board
- Eight solar panels for 12W total, 6W nominal in the sun



Launch

- Nov 19th, 8:15pm EST 2013
- 29 satellites released in less than a hour
- 28 Cubesats of various make and models
- 300 Miles above earth, Minotaur 1 rocket

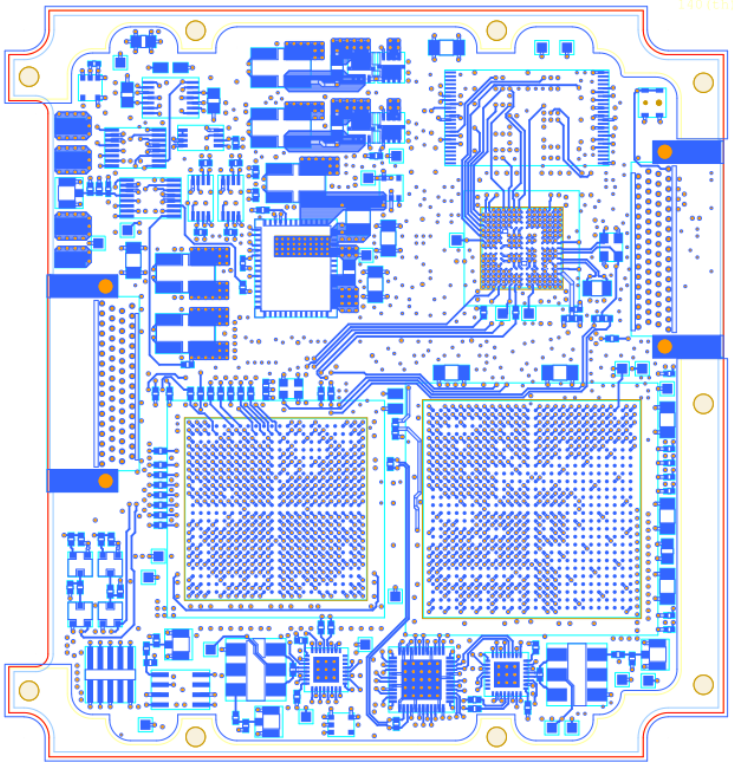
Results

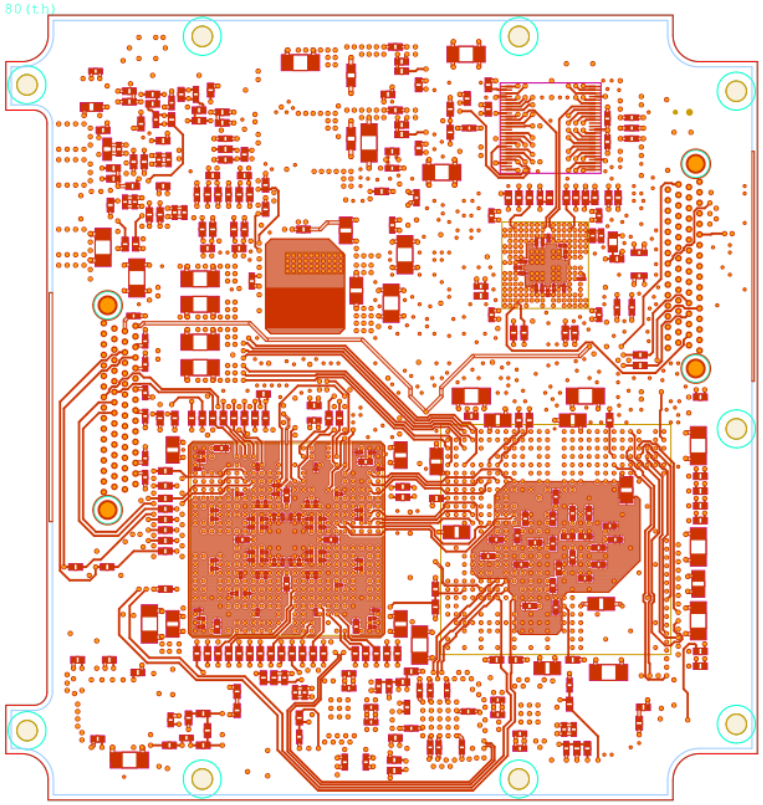
- All 8 satellites launched and able to talk to ground station.
- Late spin of Analog Radio to improve reliability – plus and minuses
- Late changes had a big impact, cold batteries
- Software has been updated on orbit – new digital radio design update has also been done on orbit
- Main software development slowly adding other features (in the last few months)
- Relatively Cheap development, quick deployment, LANL needs more experience/code for running satellites

Block II

- Update to design to overcome weaknesses in first effort.
- Double batteries and solar panels, and heater for batteries.
- Spread spectrum communication for the radio (new radio board design)
- Additional Features: Star Field Sensor, GPS, bigger reaction wheels, ...
- Increase reliability, ease of deployment and processing.

Digital Radio II





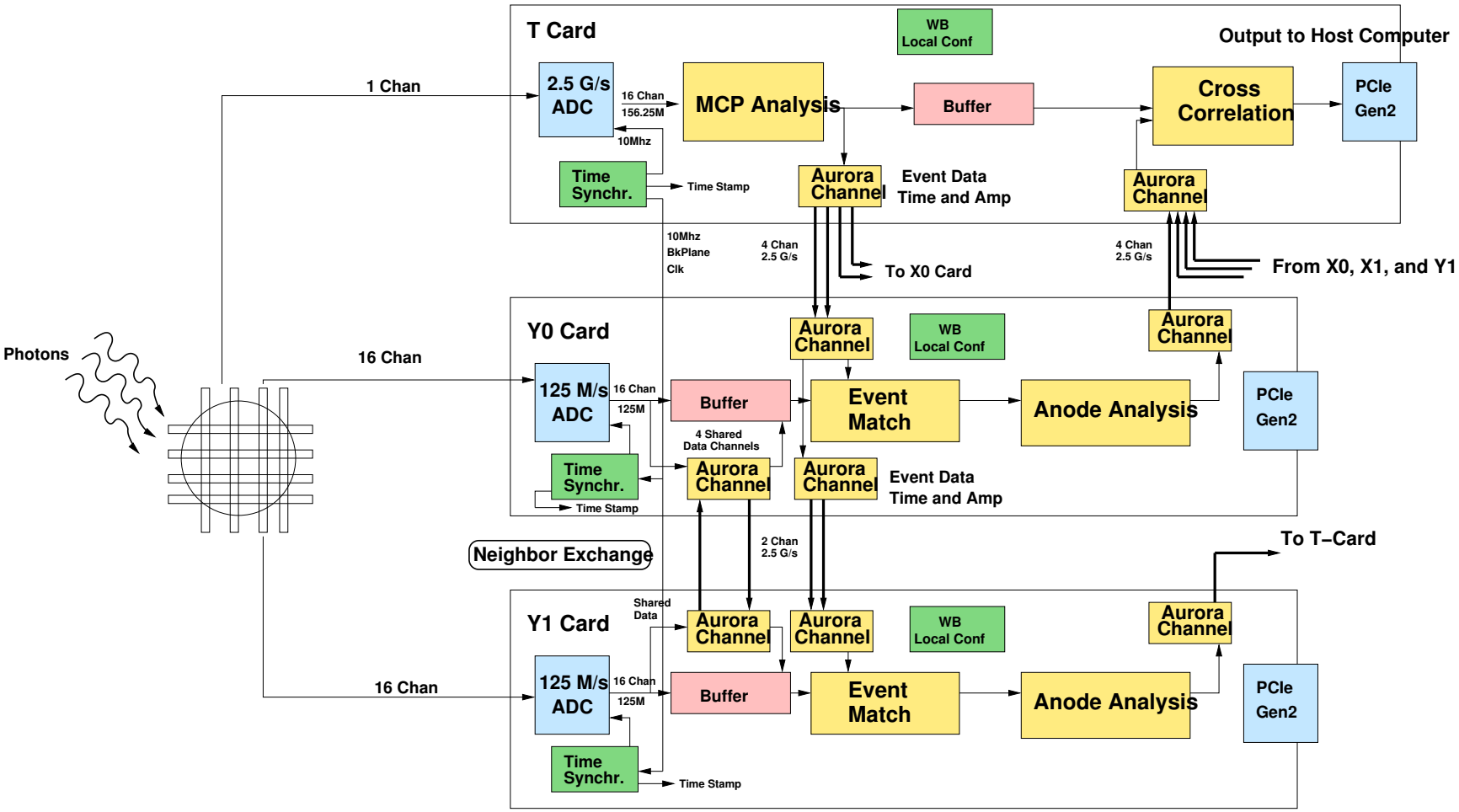
Newer Family of FPGA, larger SRAM, larger Flash, parallel ADCs and DACs.

Block II - Status

- Digital Radio boards being built (this week)
- C&DH is a still a variant of the Digital Radio board
- Power board and backplane are built
- ADCS – controls motors and sensors, in layout
- Analog Radio still under design/layout
- Most boards in layout or close to fabrication.
- Antennas, mechanical design and minor details still under development.

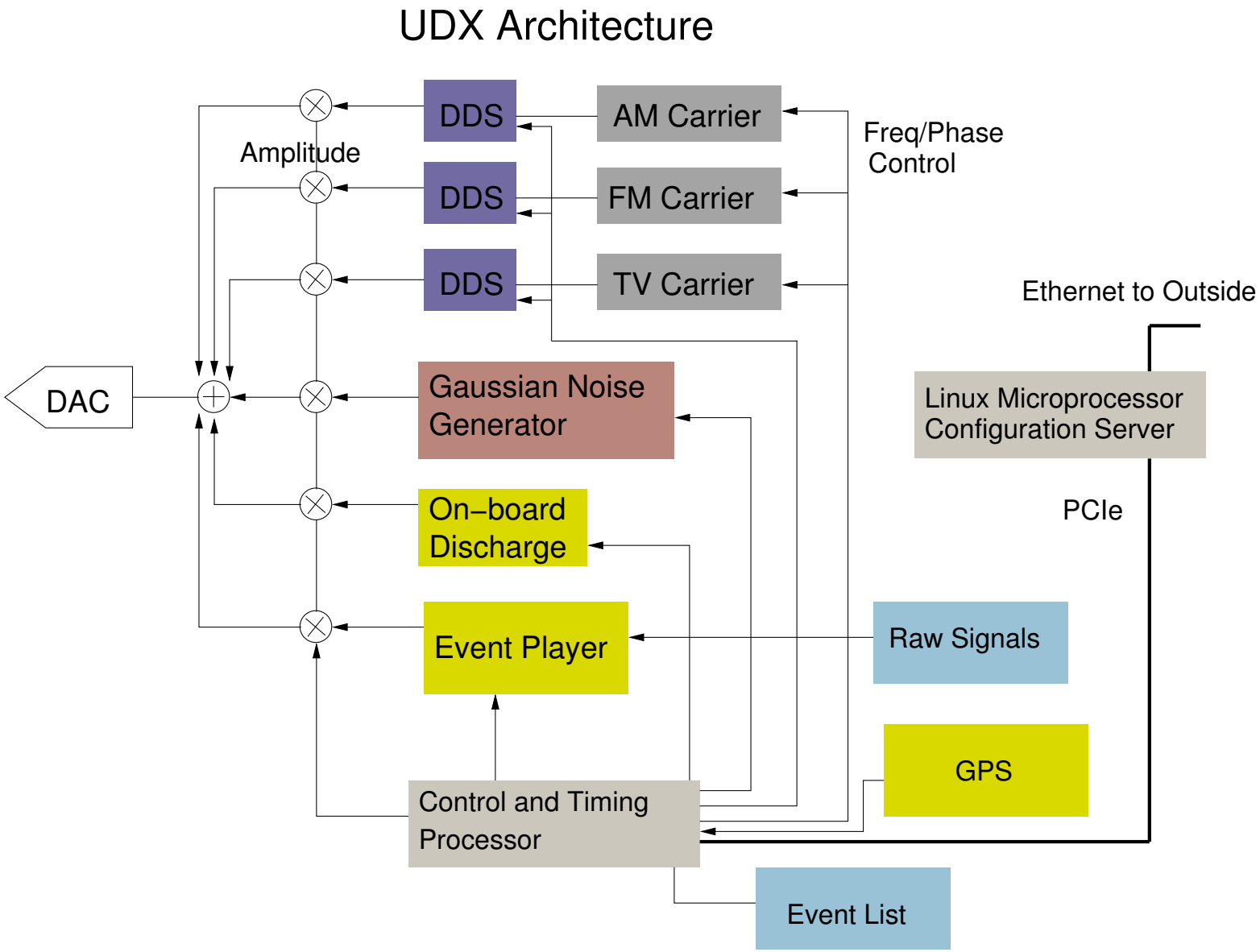
Cross Strip

Change 21GB/s of data into 100M events/s



X0 and X1 not shown, similar to above

UDX - Custom RF Generation



System Design

- What data need to move? Where and when?
- What computation is required? Where and when?
- What can be configured from SW and how?
- What role does any CPU play and what impact will that role have on the CPU?
- Does it meet the overall goals of the project or task?